IN THE SPECIFICATION:

Please amend paragraph number **[0038]** as follows:

[0038] Referring to drawing FIG. 10, the next steps in the method of the present invention are (1) forming a suitable metal coating on the glass layer 30 to substantially hermetically seal the areas of the glass layer 30 etched to expose the bond pads 14 of the semiconductor chips 12 and to form suitable electrical connections to the bond pads 14, (2) applying a suitable resist coating (not shown) to the metal coating on the glass layer 30 having the desired ~~circuitry~~ circuits 16 to connect the bond pads 14 to a predetermined desired connector (not shown), and (3) etching the metal coating to yield the desired ~~circuitry connections~~ circuits 16 (see drawing FIGs. 2 through 4) to the bond pads 14 of each semiconductor chip 12. Subsequent to the ~~circuitry~~ circuits 16 being formed on the surface of the glass layer 30 to form a substantially hermetical seal and to form connections with the bond pads 14 of semiconductor chips 12, the resist coating is removed from the circuits 16 and the individual semiconductor chips 12 are separated by sawing, severing, dividing or cutting the street areas 22 between each semiconductor chip 12 as shown at cuts 50. The cuts 50 are made in the street areas 22 so that portions of the glass layer 30 and the glass coating 40 remain in substantial contact with each edge of each semiconductor chip 12, thereby substantially hermetically sealing all edges of each semiconductor chip 12. In this manner, each semiconductor chip 12 is substantially fully hermetically sealed on the top, bottom, and all edges thereof by the glass layer 30 and the glass coating 40 and metal circuits 16 connected to bond pads 14, thereby leaving no portion of the semiconductor chip 12 exposed for any environmental attack thereto.

Please amend paragraph number **[0039]** as follows:

[0039] Referring to drawing FIG. 11, shown connected to a conventional lead frame 60 is a portion of a semiconductor chip 12 substantially fully hermetically sealed on the top thereof by glass layer 30, on the bottom thereof by glass coating 40, and all edges thereof by the combination of the glass layer 30 and the glass coating 40. As shown, a bond pad 14 having

~~circuitry~~ circuits 16 connected thereto and substantially hermetically sealing the same is connected to a lead 62 of the conventional lead frame 60 by a suitable wire connection 66 having one end thereof 68 connected to the ~~circuitry~~ circuit 16 connected, in turn, to bond pad 14 of semiconductor chip 12, while the other end 70 of the wire connection 66 is connected to the lead 62 of conventional lead frame 60. The semiconductor chip 12 is secured to or mounted on the paddle 64 of the conventional lead frame 60. Alternatively, the lead 62 of the conventional lead frame 60 may extend over (not shown) the semiconductor chip 12 for a typical lead-over-chip arrangement well known in the art with the ~~wires~~ wire connections 66 attaching the ~~circuitry~~ circuits 16 to the lead 62 in such a manner.

Please amend paragraph number **[0047]** as follows:

[0047] The ninth step of the method of the present invention comprises applying a coating of suitable resist material on the active circuitry side (top or first side) of the semiconductor chips 12 over the glass layer 30 on the wafer 10, leaving the bond ~~pad areas~~ pads 14 of the semiconductor chips 12 free of resist material. Any suitable resist material may be used, depending upon the desired process parameters of the etching process to be used.

Please amend paragraph number **[0048]** as follows:

[0048] As the tenth step of the method of the present invention, subsequent to applying the resist coating over the glass layer 30, the glass layer 30 is etched through to uncover predetermined bond ~~pad areas~~ pads 14 of each semiconductor chip 12 of the wafer 10. Any suitable etching process may be used, depending upon the type of glass layer 30 applied to the active circuitry side of the wafer 10.

Please amend paragraph number **[0054]** as follows:

[0054] As the sixteenth step of the method of the present invention, portions of the street areas 22 located between the semiconductor chips 12 of the wafer 10 are sawed through at ~~locations~~ cuts 50 in the street areas 22 so that glass layer 30 and glass coating 40 are maintained

on the edges of each semiconductor chip 12 and the active circuitry (top or first) side of the semiconductor chip 12 and the bottom (second side) of the semiconductor chip 12, thereby substantially hermetically sealing the semiconductor chip 12 in glass while the bond pads 14 are substantially hermetically sealed by the metal coating forming the desired circuits 16 connected thereto. In this manner a plurality of semiconductor chips 12 have been formed with each semiconductor chip 12 being substantially fully hermetically sealed on each side thereof and on each edge thereof and the bond pads 14 being substantially hermetically sealed by the metal coating forming the circuits 16 to prevent environmental corrosion thereof without the use of a separate package. By using the method of the present invention to substantially fully hermetically seal the semiconductor chip 12, without the use of a separate package, the semiconductor chip 12 of the present invention is of minimum size and occupies a minimum volume. Also, the semiconductor chip 12 formed by the method of the present invention has a desired configuration of circuitry connecting the bond pads 14 of the semiconductor chip 12 to a desired connector configuration which may include conventional lead frames 60 or lead-over-chip frames. If connected to lead frames, the semiconductor chip 12 of the present invention which is fully hermetically sealed in glass layer 30 and glass coating 40 may be subsequently packaged in suitable plastic materials in a conventional manner for further protection from damage. If desired, since the semiconductor chips 12 are substantially fully hermetically sealed by glass layer 30, having the desired ~~circuitry~~ circuits 16 thereon, and glass coating 40, the semiconductor chips 12 may be directly inserted into mating connectors which match the circuitry formed on the semiconductor chips 12.

Please amend paragraph number **[0057]** as follows:

[0057] Additionally, since the semiconductor chips 12 are substantially fully hermetically sealed having suitable ~~circuitry~~ circuits 16 formed thereon, the semiconductor chips 12 are easily tested in their final form for determining if the individual semiconductor chips 12 are known-good-die ready for use.